ALPHA DATA

ADC-PCIE-XMC
User Manual

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	Head Office	US Office
Address:	4 West Silvermills Lane, Edinburgh, EH3 5BD, UK	611 Corporate Circle Suite H Golden, CO 80401
Telephone:	+44 131 558 2600	(303) 954 8768
Fax:	+44 131 558 2700	(866) 820 9956 - toll free
email:	sales@alpha-data.com	sales@alpha-data.com
website:	http://www.alpha-data.com	http://www.alpha-data.com

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1 About the Hardware

The ADC-PCIE-XMC is a half-length PCI Express compliant XMC carrier designed to host Alpha Data ADM-XRC series of FPGA mezzanine cards.

The ADC-PCIE-XMC is compatible with PCIe Gen2 and lower.

This carrier supports ADM-XRC series cards utilizing Virtex 6 and newer FPGAs.

The ADC-PCIE-XMC also supports the optional P4 auxiliary IO connector available on most Alpha Data mezzanine cards.

Two PCIe redriver components ensure that a high integrity link is maintained at all PCI express operation speeds while forcing either x8 or x4 link widths.

Redundant power ORing selects between the PCIe edge and the external power connector to ensure the appropriate 12V power is being applied o the XMC site.

1.1 Architecture

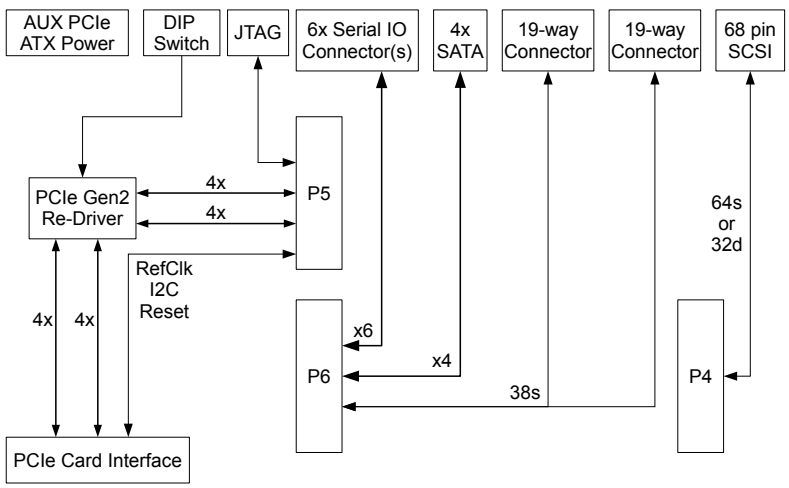

Figure 1 : ADC-PCIE-XMC Block Diagram

1.2 Board Features

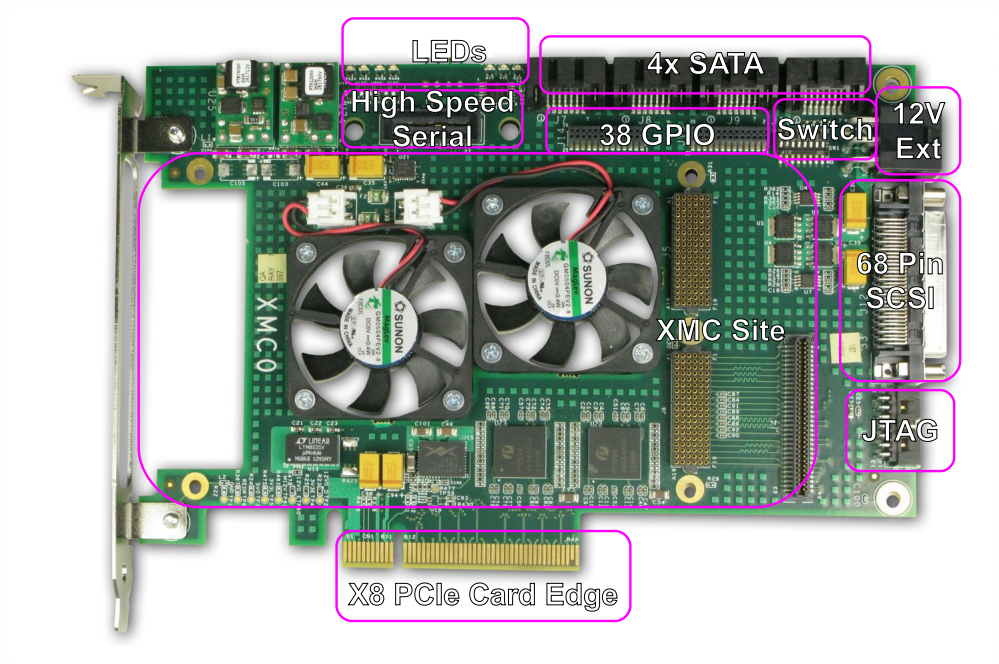

Figure 2 : Features

1.3 Limits and Measurements

The ADC-PCIE-XMC is a standard 1/2 length PCI express plugin card adhering to the PCI Express Card Electromechanical Specification.

Dimension	Measurement
X PCB	167.7mm
X PCB + J12 (SCSI)	173.6mm
Y	111.2mm
Z above PCB (max with XMC)	14.47mm
Z below PCB (max with XMC)	2.67mm
Z PCB thickness	1.57mm
Weight	100g

Table 1 : Measurements

Supply	Limit
Total Power (with XMC Card)	25W
Max Required Carrier Power	5.2W
Typical Required Carrier Power	2.8W
VPWR (12V) to XMC site without Aux Connector	2.1A
VPWR (12V) to XMC site with AUX connector	8A
3V3 (to XMC site)	4A
M12V (to XMC site)	1A
3V3 Aux (to XMC site)	20mA

Table 2 : Power and Current Limits

Note:
The total power consumption of 25W is based on the PCIe card specification. This number can be exceeded if extra care is taken to cool the ADC-PCIE-XMC and associated FPGA card in a non-standard chassis.

1.4 DIP Switch (SW1)

The ADC-PCIE-XMC has a single 8 position DIP switch which controls the following functions.

Switch Index	Function	Off Position	On Position
1	Non-Volatile Memory Read Only	Read/Write	Read Only
2	XMC Address index 0	0	1
3	XMC Address index 1	0	1
4	XMC Address index 2	0	1
5	Bottom x4 Disable	Bottom 4 lanes Enabled	Bottom 4 lanes Disabled
6	Bottom x4 Loop Back	Normal Operation	Loop Back Re-Driver
7	Top x4 Disable	Top 4 lanes Enabled	Top 4 lanes Disabled
8	Top x4 Loop Back	Normal Operation	Loop Back Re-Driver

Table 3 : Switch (SW1)

Note:
PCIe lane width of 4 Requires SW1-5 OFF, SW1-7 ON

Note:
PCIe lane width of 8 Requires SW1-5 OFF, SW1-7 OFF

1.5 LEDs

Three status LEDs display the condition of the redundant power ORing circuitry.

LED	Color	Status When Lit
D3	RED	Fault at External 12V Connector
D2	RED	Fault at PCIe Card Edge
D1	GREEN	Power OK

Table 4 : LEDs

Four status LEDs display the condition of the PCIe link.

LED	Color	Status When Lit
D4	GREEN	Signal detect on bottom four lanes from FPGA to Motherboard
D5	GREEN	Signal detect on bottom four lanes from Motherboard to FPGA
D6	GREEN	Signal detect on top four lanes from FPGA to Motherboard
D7	GREEN	Signal detect on top four lanes from Motherboard to FPGA

Table 5 : LEDs

1.6 XMC Site

An XMC card may be fitted here with its IO area accessible externally though the rear panel.

1.7 PCIe Power Connector

This connector may be connected to the system's power supply using a standard 6-pin PCIe power cable to increase the available power to the XMC site.

1.8 Power Regulation

3.3V and -12.0V to the XMC site are generated from the +12.0V supply from the PCIe power connector or card edge.

The 3.3V power from the card edge is used to power the PCIe re-drivers.

1.9 Connector Descriptions

The ADC-PCIE-XMC is populated with a variety of connectors that help developers break out both high-speed and GPIO signals of the XMC FPGA Card.

1.9.1 XMC Site (J4, J5, J6)

The ADC-PCIE-XMC supports a single XMC card with an optional PN4 connector. This XMC site is fully compliant with VITA 42.0. There are two 40mm Fans directly under the XMC site to help cool the mezzanine card.

1.9.2 High-Speed Serial IO (J11)

The ADC-PCIE-XMC uses a high-speed connector to distribute the high-speed signals from XMC connector J6. This connector a samtec QSE-014-F-D-DP that supports PCB retention of the plug connector.

1.9.3 SATA (J7, J8, J9, J10)

The ADC-PCIE-XMC has four standard right angle SATA receptacles for use with SATA compliant storage devices. Alpha Data offers IP to interface between Alpha Data XMC cards and mass storage devices.

1.9.4 SCSI (J12)

The ADC-PCIE-XMC hosts a 68 Pin industry standard SCSI connector. This interface is intended to be used for LVCMOS, LVDS, or any other electrical standard compliant with the XMC target FPGA.

This connector mates with Molex 71425-3001, VHDCI Plug Kit.

1.9.5 38 GPIO (J13, J14)

The ADC-PCIE-XMC has two GPIO connectors for accessing the 38 3.3V CMOS signals available from XMC site J6. These connectors are pin-compatible with the GPIO interface of the Alpha Data ADC-XMC-II carrier.

This connector is a Samtec part number FLE-113-01-G-DV and has multiple mating options which can be found at www.samtec.com.

1.9.6 JTAG (J2)

A JTAG interface compatible with Xilinx a 14-pin parallel cable is available at the rear of the card. This interface can be used for debugging and standalone programming of XMC cards.

1.9.7 External 12V Power (J3)

A standard 6-pin 12V0 PCIe ATX power supply jack is available for applications which require more power than can be delivered over the PCIe Card Edge.

2 Connector Pin Assignments

2.1 J4 <-> J12

Signal	J4 Pin	J12 Pin		J12 Pin	Signal	Signal
GND	-	1	|	35	-	GND
J4_1_P	1	2	|	18	33	J4_17_P
J4_1_N	3	36	|	52	35	J4_17_N
J4_2_P	2	3	|	19	34	J4_18_P
J4_2_N	4	37	|	53	36	J4_18_N
J4_3_P	5	4	|	20	37	J4_19_P
J4_3_N	7	38	|	54	39	J4_19_N
J4_4_P	6	5	|	21	38	J4_20_P
J4_4_N	8	39	|	55	40	J4_20_N
J4_5_P	9	6	|	22	41	J4_21_P
J4_5_N	11	40	|	56	43	J4_21_N
J4_6_P	10	7	|	23	42	J4_22_P
J4_6_N	12	41	|	57	44	J4_22_N
J4_7_P	13	8	|	24	45	J4_23_P
J4_7_N	15	42	|	58	47	J4_23_N
J4_8_P	14	9	|	25	46	J4_24_P
J4_8_N	16	43	|	59	48	J4_24_N
J4_9_P	17	10	|	26	49	J4_25_P
J4_9_N	19	44	|	60	51	J4_25_N
J4_10_P	18	11	|	27	50	J4_26_P
J4_10_N	20	45	|	61	52	J4_26_N
J4_11_P	21	12	|	28	53	J4_27_P
J4_11_N	23	46	|	62	55	J4_27_N
J4_12_P	22	13	|	29	54	J4_28_P
J4_12_N	24	47	|	63	56	J4_28_N
J4_13_P	25	14	|	30	57	J4_29_P
J4_13_N	27	48	|	64	59	J4_29_N
J4_14_P	26	15	|	31	58	J4_30_P
J4_14_N	28	49	|	65	60	J4_30_N
J4_15_P	29	16	|	32	61	J4_31_P
J4_15_N	31	50	|	66	63	J4_31_N
J4_16_P	30	17	|	33	62	J4_32_P
J4_16_N	32	51	|	67	64	J4_32_N
GND	-	34	|	68	-	GND

Table 6 : J4 to J12

Note: All signals designated as a P/N pair are routed with 100 ohm differential tracks from supported FPGA cards to the connectors on the ADC-PCIE-XMC

2.2 J6 <-> J11

Signal	J11 Pin	J6 Pin		J6 Pin	J11 Pin	Signal
J6_TX4_P	1	A5	|	A15	2	J6_RX4_P
J6_TX4_N	3	B5	|	B15	4	J6_RX4_N
J6_TX5_P	5	D5	|	D15	6	J6_RX5_P
J6_TX5_N	7	E5	|	E15	8	J6_RX5_N
J6_TX6_P	17	A7	|	A17	18	J6_RX6_P
J6_TX6_N	19	B7	|	B17	20	J6_RX6_N
J6_TX7_P	21	D7	|	D17	22	J6_RX7_P
J6_TX7_N	23	E7	|	E17	24	J6_RX7_N
J6_TX8_P	9	A9	|	A19	10	J6_RX8_P
J6_TX8_N	11	B9	|	B19	12	J6_RX8_N
J6_TX9_P	13	D9	|	D19	14	J6_RX9_P
J6_TX9_N	15	E9	|	E19	16	J6_RX9_N

Table 7 : J6 to J11

2.3 J6 <-> J7,J8,J9,J10

Signal	SATA Con.Pin	J6 Pin		J6 Pin	SATA Pin	Signal
J6_TX0_P	J7.2	A1	|	A11	J7.6	J6_RX0_P
J6_TX0_N	J7.3	B1	|	B11	J7.5	J6_RX0_N
J6_TX1_P	J8.2	D1	|	D11	J8.6	J6_RX1_P
J6_TX1_N	J8.3	E1	|	E11	J8.5	J6_RX1_N
J6_TX2_P	J9.2	A3	|	A13	J9.6	J6_RX2_P
J6_TX2_N	J9.3	B3	|	B13	J9.5	J6_RX2_N
J6_TX3_P	J10.2	D3	|	D13	J10.6	J6_RX3_P
J6_TX3_N	J10.3	E3	|	E13	J10.5	J6_RX3_N

Table 8 : J6 to J7,J8,J9,J10

2.4 J6 <-> J13,J14

Signal	J6 Pin	J14 Pin		J13 Pin	J6 Pin	Signal
GND	-	1	|	1	-	GND
GND	-	2	|	2	-	GND
GPIO_SC_0	C1	3	|	3	F1	GPIO_FC_0
GPIO_SC_1	C2	4	|	4	F2	GPIO_FC_1
GPIO_SC_2	C3	5	|	5	F3	GPIO_FC_2
GPIO_SC_3	C4	6	|	6	F4	GPIO_FC_3
GPIO_SC_4	C5	7	|	7	F5	GPIO_FC_4
GPIO_SC_5	C6	8	|	8	F6	GPIO_FC_5
GPIO_SC_6	C7	9	|	9	F7	GPIO_FC_6
GPIO_SC_7	C8	10	|	10	F8	GPIO_FC_7
GPIO_SC_8	C9	11	|	11	F9	GPIO_FC_8
GPIO_SC_9	C10	12	|	12	F10	GPIO_FC_9
GND	-	13	|	13	-	GND
GND	-	14	|	14	-	GND
GPIO_SC_10	C11	15	|	15	F11	GPIO_FC_10
GPIO_SC_11	C12	16	|	16	F12	GPIO_FC_11
GPIO_SC_12	C13	17	|	17	F13	GPIO_FC_12
GPIO_SC_13	C14	18	|	18	F14	GPIO_FC_13
GPIO_SC_14	C15	19	|	19	F15	GPIO_FC_14
GPIO_SC_15	C16	20	|	20	F16	GPIO_FC_15
GPIO_SC_16	C17	21	|	21	F17	GPIO_FC_16
GPIO_SC_17	C18	22	|	22	F18	GPIO_FC_17
GPIO_SC_18	C19	23	|	23	F19	GPIO_FC_18
No Connect	-	24	|	24	-	No Connect
GND	-	25	|	25	-	GND
GND	-	26	|	26	-	GND

Table 9 : J6 to J13,J14

3 Debug PCB

Each ADC-PCIE-XMC comes with a debug PCB that can be attached directly onto the low speed IO connectors J13 and J14. Developers can solder desired connections directly to the debug PCB.

All custom connections to the debug PCB should be fitted from the top side of the board (where the dual in line headers are not visible). Connections should be soldered on the bottom side of the board (the side with the connectors that mate with the ADC-XMC-II)

Snip off any extra wire or excessive solder. This PCB has minimal clearance above the SATA connectors.

The image below shows the pin mapping from the debug PCB to the XMC J6 GPIO pins.

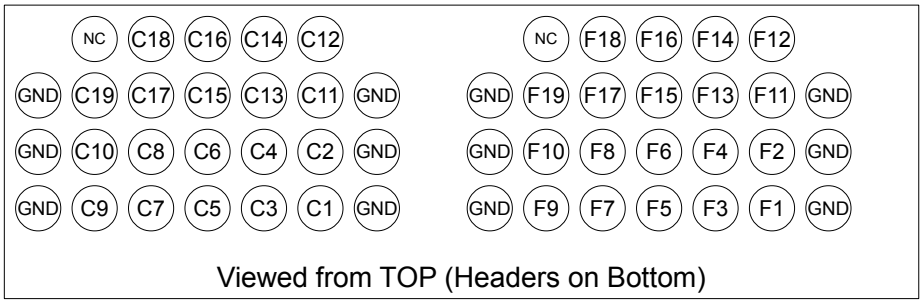

Figure 3 : Debug PCB

4 References & Specifications

ANSI/VITA 42.0	XMC Standard, December 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 42.3	XMC PCI Express® Protocol Layer Standard, June 2006, VITA, ISBN 1-885731-43-4
ANSI/IEEE 1386-2001	IEEE Standard for a Common Mezzanine Card (CMC) Family, October 2001, IEEE, ISBN 0-7381-2829-5

Table 10 : References

Revision History

Date	Revision	Changed By	Nature of Change
18 Sep 2012	0.1	K. Roth	Initial Draft
5 Dec 2012	1.0	K. Roth	Initial Release
21 Jun 2013	2.0	K. Roth	Incorporated changes to revision 2 PCB (Re-drivers, onboard voltage regulation, and debug PCB).
7 Oct 2013	2.1	K. Roth	Swapped LED desicription D1 and D3.
14 Jan 2015	2.2	K. Roth	Updated J4 <-> J12 table and added note about differential routing.
4 Dec 2015	2.3	K. Roth	The PCIe speed specs have been reduced to gen2 to support alternate re-driver parts.
16 Mar 2018	2.4	K. Roth	Updated debug header diagram to increase numerical references by 1 to match J6 properly.

Address: 4 West Silvermills Lane,
Edinburgh, EH3 5BD, UK
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Fax: +44 131 558 2700
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website: http://www.alpha-data.com

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Telephone: (303) 954 8768
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